

Relay Timer

Description

The U2101B monolithic integrated bipolar circuit is a versatile timer device for relay control. Because of two

integrated, freely connectable operational amplifiers, it covers a very wide range of applications.

Features

- Adjustable window for trigger input
- Enable input for triggering
- Adjustable noise suppression
- Adjustable and retriggerable tracking time
- Enable and block delay
- Two integrated operational amplifiers – freely connectable
- 100 mA relay driver

Applications

- Motion detectors
- Tracking controllers
- Multiple timer
- Conditional switches
- Clock generators

Case: DIP 16, SO 16

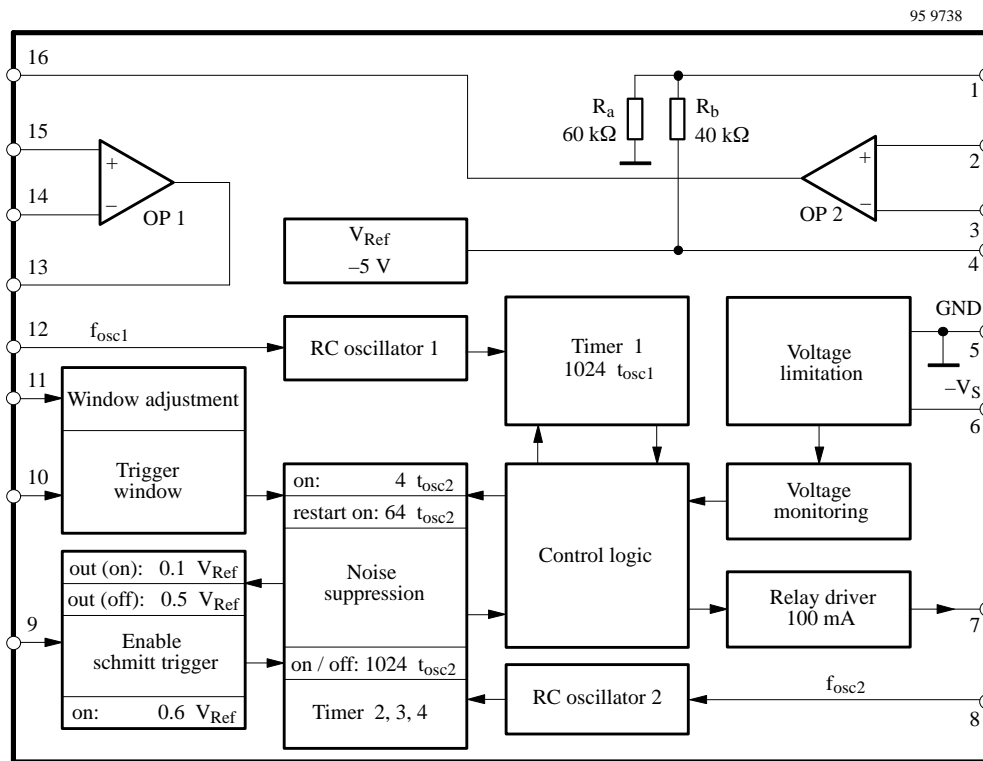


Figure 1. Block diagram

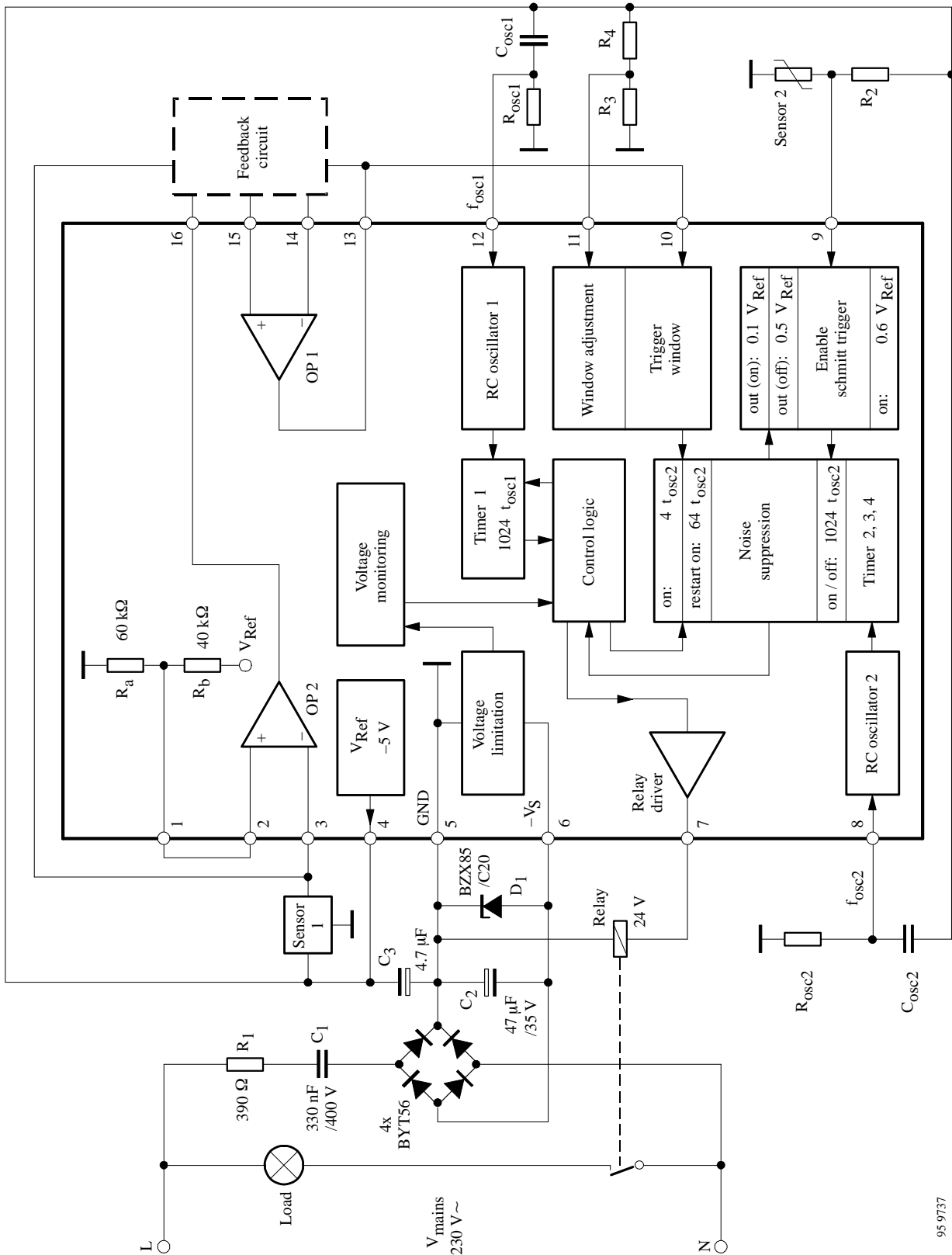
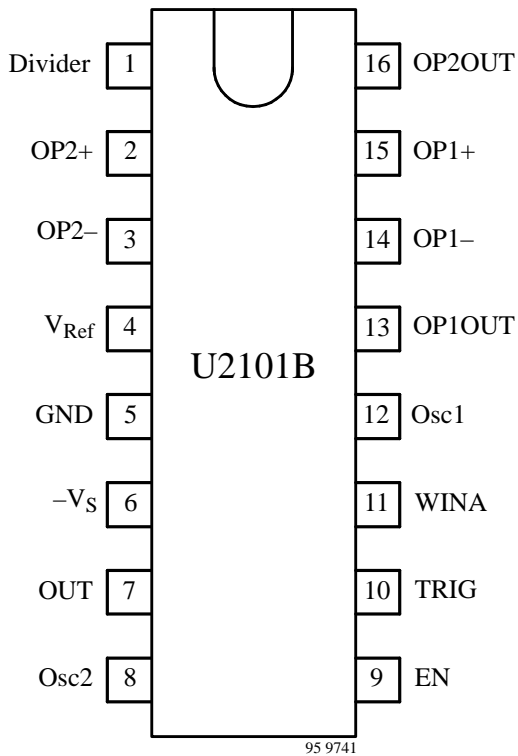


Figure 2. Block diagram with typical circuit

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Pin Description



Pin	Symbol	Function
1	Divider	Voltage divider
2	OP2+	Non-inverting input OP2
3	OP2-	Inverting input OP2
4	V _{Ref}	Reference voltage -5V
5	GND	Ground
6	-V _S	Supply voltage
7	OUT	Output
8	Osc2	RC oscillator 2 (noise suppression)
9	EN	Enable input
10	TRIG	Trigger input
11	WINA	Trigger window adjustment
12	Osc1	RC oscillator 1 (tracking time)
13	OP1OUT	Output OP1
14	OP1-	Inverting input OP1
15	OP1+	Non-inverting input OP1
16	OP2OUT	Output OP2

Supply, Pin 6

The voltage limitation in U2101B allows a simple capacitive supply which is derived from the mains voltage via a bridge rectifier (see figure 3).

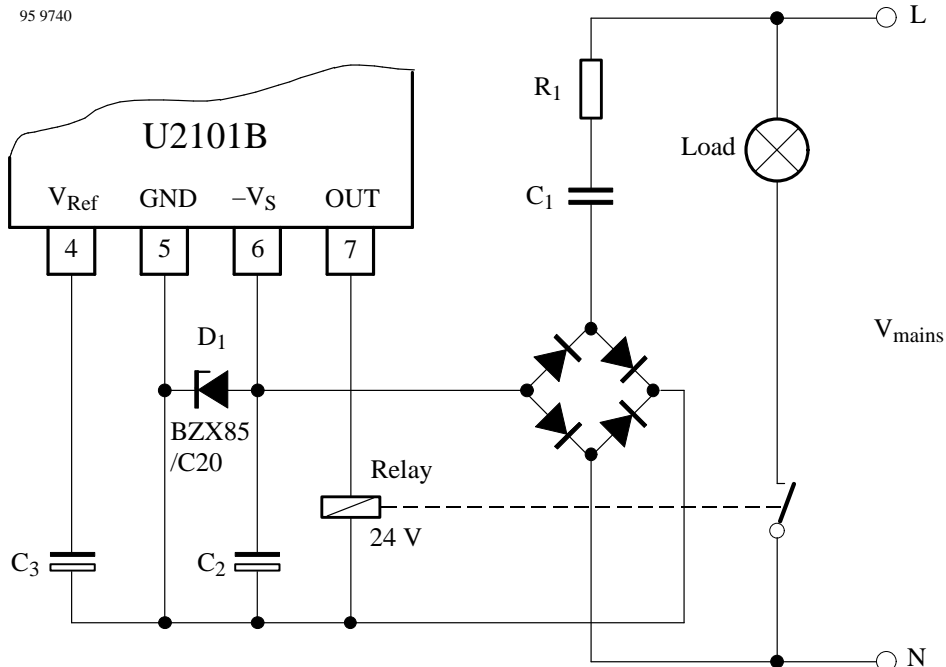


Figure 3. Supply

U2101B

Capacitor C_1 is calculated as follows:

$$X_{C1} = 0.85 \times \frac{V_{\text{mains}} - V_S}{I_{\text{tot}}}$$

where

$$I_{\text{tot}} = I_S + I_{\text{Rel}} + I_X$$

I_S = current consumption of the IC without load

I_{Rel} = relay current

I_X = current consumption of the external components

$$C_1 = \frac{1}{\omega \times X_{C1}}$$

The following applies for R_1 :

$$R_1 \approx \frac{1}{10} X_{C1}$$

At Pin 4, the circuit provides a stabilized reference voltage of -5 V.

Voltage Monitoring

While the operating voltage is being built up and reduced, uncontrolled states and activation of the output stage are prevented by the internal monitoring circuit. All latches in the circuit, the divider and the control logic are reset.

After the supply voltage is applied, a single operating cycle is started independently of the trigger inputs in order to immediately make the entire function visible.

Trigger Inputs, Pins 9 and 10

The trigger condition for the time stage is determined by the two inputs Pins 9 and 10. To initiate a triggering operation, both inputs must be in the ON state, since they are equivalent and AND connected. The tracking time begins when the trigger condition finishes. The output remains in the ON state until the tracking time is over.

The enable input, Pin 9, is designed as a comparator with hysteresis. The blocking threshold is switched over by the noise suppression in order to avoid faults as a result of load switching (see figure 4).

The trigger input, Pin 10, is designed as a window discriminator. The window is adjusted at Pin 11. When $V_{11} = V_4$, the minimum window of approximately 250 mV is set. When $V_{11} = V_5$, the maximum window is approximately 1 V. The window discriminator is in the OFF state when the voltage at Pin 10 is within the window set at Pin 11 (see figure 5).

If a resistor divider with a NTC resistor is connected at Pin 11, it is possible to compensate for the temperature dependence of an IR sensor, for example. This means that the range becomes temperature independent.

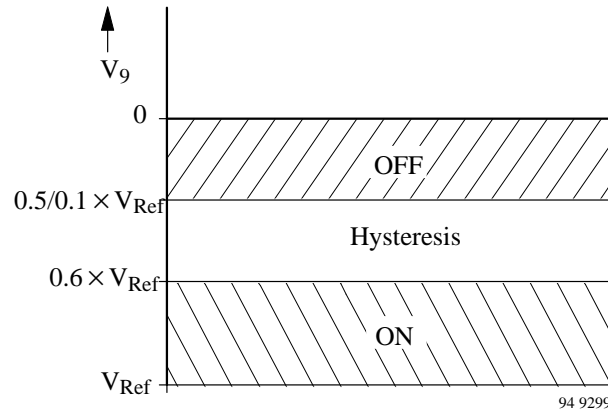


Figure 4. Trigger condition, Pin 9

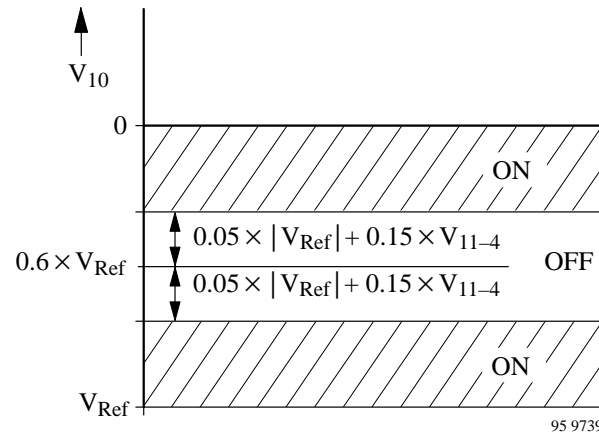


Figure 5. Trigger condition, Pin 10

Noise Suppression, Pin 8

The internal noise suppression ensures that peak noise signals at the inputs do not cause undesired triggering. Also, triggering is prevented for a certain time after the load is switched off in order to avoid any intrinsic fault. The delay times are derived from oscillator 2 at Pin 8, the frequency, $f_{\text{osc}2}$, of which is calculated as follows:

$$f_{\text{osc}2} = \frac{1}{1.6 \times R_{\text{osc}2} \times C_{\text{osc}2}},$$

whereas

$C_{\text{osc}2}$ should not be greater than 1 μF .

This gives the period duration $t_{\text{osc}2}$:

$$t_{\text{osc}2} [\text{s}] = 1600 \times R_{\text{osc}2} [\text{k}\Omega] \times C_{\text{osc}2} [\mu\text{F}]$$

The enable input, Pin 9, is buffered for $1024 \times t_{\text{osc}2}$ during switching on and switching off, and the input of the window discriminator at Pin 10 is buffered for $4 \times t_{\text{osc}2}$ during switching on and for $64 \times t_{\text{osc}2}$ in the case of switching back on. Appropriately selecting $R_{\text{osc}2}$ and $C_{\text{osc}2}$ at Pin 8 allows any delay times to be adjusted so that can be adapted to the respective requirements.

RC Oscillator 1, Pin 12

The oscillator 1 with the following divider stage 1:1024 allows a very long and reproducible tracking time t_t . The circuitry of Pin 12 for a certain tracking time t_t can be calculated as follows:

$$R_{osc1} \text{ [k}\Omega\text{]} = \frac{t_t \text{ [s]} \times 10^3}{1.6 \times 1024 \times C_{osc1} \text{ [}\mu\text{F]}}$$

$$C_{osc1} \text{ [k}\Omega\text{]} = \frac{t_t \text{ [s]} \times 10^3}{1.6 \times 1024 \times R_{osc1} \text{ [}\mu\text{F]}}$$

whereas C_{osc1} should not be greater than $1\mu\text{F}$.

Voltage Divider, Pin 1

Two freely connectable operational amplifiers, OP1 and OP2, are used to evaluate several sensor signals. The tap of a voltage divider between GND and V_{Ref} with a voltage level of $0.6 \times V_{Ref}$ is available at Pin 1. The middle of the discriminator window is also at this value. Assuming that the output of one operational amplifier is connected at the trigger input, Pin 10 (window discriminator), the dc operating point of this operational amplifier can be adjusted without additional external resistors by connecting the input to Pin 1. This value is approximately in the center of the OP control range.

Absolute Maximum Ratings

Reference point Pin 5, unless otherwise specified

Parameters	Symbol	Value	Unit
Power supply			
Current	Pin 6	$-I_S$	15 mA
$t < 10 \mu\text{s}$	Pin 6	$-i_S$	60 mA
Reference voltage source			
Output current	Pin 4	I_O	5 mA
Output stage			
Output voltage	Pin 7	$-V_O$	V_S to 1.8 V
Input currents	Pin 13 and 16	$\pm I_I$	5 mA
Input voltages	Pins 1, 2, 3, 8, 9, 10, 11, 12, 14, 15	V_I	V_{Ref} to 0 V
Storage temperature range	T_{stg}	-40 to +125	$^{\circ}\text{C}$
Junction temperature	T_j	+125	$^{\circ}\text{C}$
Ambient temperature	T_{amb}	-10 to +100	$^{\circ}\text{C}$

Thermal Resistance

Parameters	Symbol	Maximum	Unit
Junction ambient			
DIP 16	R_{thJA}	120	K/W
SO 16 on PC board		180	
SO 16 on ceramic		100	

Electrical Characteristics

$V_S = -18\text{ V}$, $T_{\text{amb}} = 25^\circ\text{C}$, reference point Pin 5, unless otherwise specified

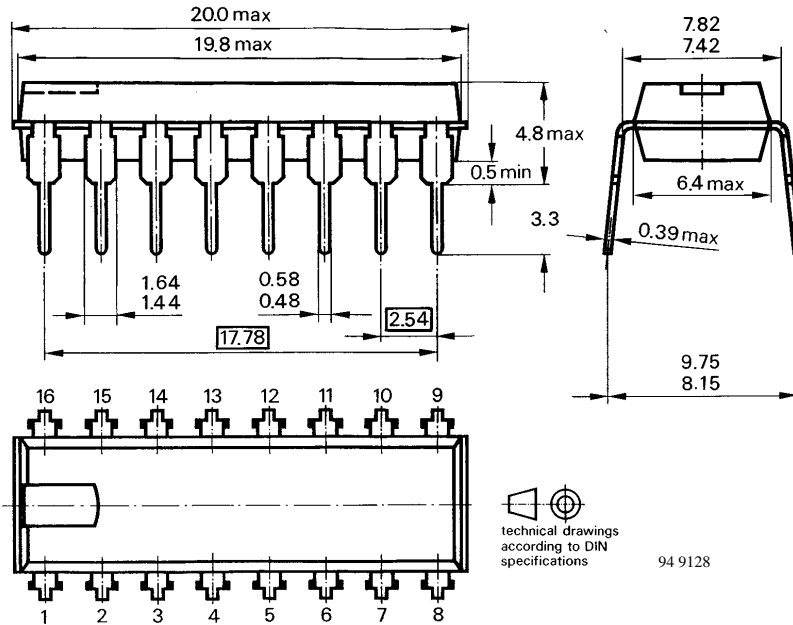
Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Supply voltage limitation	$I_S = 2\text{ mA}$ Pin 6	$-V_S$	20.5	22	23.5	V
	$I_S = 5\text{ mA}$ Pin 6	$-V_S$	20.6	22.1	24	
Current consumption	$V_S = -18\text{ V}$, output stage OFF $V_3 < V_2$, $V_{14} < V_{15}$ Pin 6	$-I_S$			1.75	mA
	$V_3 > V_2$, $V_{14} > V_{15}$ Pin 6	$-I_S$			4	
Voltage monitoring Pin 6						
Switch-on threshold		$-V_{\text{Son}}$	13.5	15	16.5	V
Switch-off threshold		$-V_{\text{Soff}}$	5	6.5	7.5	
Reference voltage	$I_4 = 0.1\text{ mA}$ Pin 4	$-V_{\text{Ref}}$	4.75	5	5.25	V
	$I_4 = 3\text{ mA}$ Pin 4	$-V_{\text{Ref}}$	4.55	5	5.25	
Voltage divider reference point Pin 4 Pin 1						
Voltage divider resistor R_a		R_a	45	60	75	k Ω
Voltage divider resistor R_b		R_b	30	40	50	k Ω
Resistance ratio		R_a/R_b	1.45	1.5	1.55	–
Output voltage		V_O	1.75	2	2.25	V
Window discriminator reference point Pin 4						
Input current	$V_4 < V_{10} < V_5$ Pin 10	I_I		0.1	0.5	μA
Upper threshold	Pins 10 and 11	V_{TU}	$0.45 V_{\text{Ref}} + 0.15 V_{11}$			
Lower threshold	Pins 10 and 11	V_{TL}	$0.35 V_{\text{Ref}} - 0.15 V_{11}$			
Input current window adjustment	$V_4 < V_{11} < V_5$ Pin 11	I_I		0.2	0.7	μA
Minimum window: Lower threshold	$V_{11} = V_4$ Pin 10	V_{TL1}	1.55	1.75	1.95	V
			Upper threshold	V_{TU1}	2.05	
Maximum window: Lower threshold	$V_{11} = V_5$ Pin 10	V_{TL2}	0.8	1	1.2	V
			Upper threshold	V_{TU2}	2.6	
Delay time	Switch-on Pin 10–7	$t_d(\text{ON1})$		$4 \cdot t_{\text{osc2}}$		s
	Restart-on	$t_d(\text{ON2})$		$64 \cdot t_{\text{osc2}}$		
Enable Schmitt trigger reference point Pin 4 Pin 9						
Input current	$V_4 < V_9 < V_5$	I_I		0.1	0.5	μA
Threshold ON		$V_{\text{T1}}/V_{\text{Ref}}$	0.38	0.4	0.42	–
Threshold OFF (off-state)		$V_{\text{T2}}/V_{\text{Ref}}$	0.47	0.5	0.53	–
Threshold OFF (on-state)		$V_{\text{T3}}/V_{\text{Ref}}$	0.87	0.9	0.93	–
Delay time	Switch-on Pin 9–7	$t_d(\text{ON})$		$1024 \cdot t_{\text{osc2}}$		s
	Switch-off	$t_d(\text{OFF})$		$1024 \cdot t_{\text{osc2}}$		
Output stage reference point Pin 6						
Saturation voltage	$I_7 = 40\text{ mA}$ Pin 7	V_{Sat}			2	V
Output current	$V_7 = V_5$ ($t < 1\text{ ms}$) Pin 7	I_O	100			mA

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Oscillator 1, t_{osc1} reference point Pin 4 Pin 12						
Input current	$V_4 < V_{12} < V_{TU}$	I_I			0.1	μA
Upper threshold		V_{TU}/V_{Ref}	0.75	0.8	0.85	–
Lower threshold		V_{TL}		0.3	0.5	V
Operating current range		I_I	2		1800	μA
Discharge current		I_{dis}	5			mA
Oscillator 2, t_{osc2} reference point Pin 4 Pin 8						
Input current	$V_4 < V_8 < V_{TU}$	I_I			0.1	μA
Upper threshold		V_{TU}/V_{Ref}	0.75	0.8	0.85	–
Lower threshold		V_{TL}		0.3	0.5	V
Operating current range		I_I	2		1800	μA
Discharge current		I_{dis}	5			mA
Operational amplifier reference point Pin 4 Pins 2, 3, 14 and 15						
Input current		I_I		25	75	nA
Input offset current		I_{IO}		2.5	25	nA
Input offset voltage		V_{IO}		2	7	mV
Temp. coefficient V_{IO}		dV_{IO}/dT		7		$\mu\text{V}/\text{K}$
Common-mode input voltage range		V_{ICR}	0.1		3	V
Output current	$V_O = 2.5 \text{ V}$ Pins 13 and 16	$\pm I_O$	1			mA
Output voltage: Lower limit Upper limit	$I_O = 100 \mu\text{A}$ Pins 13 and 16	V_{OL} $-V_{OU}$			0.9 1.6	V

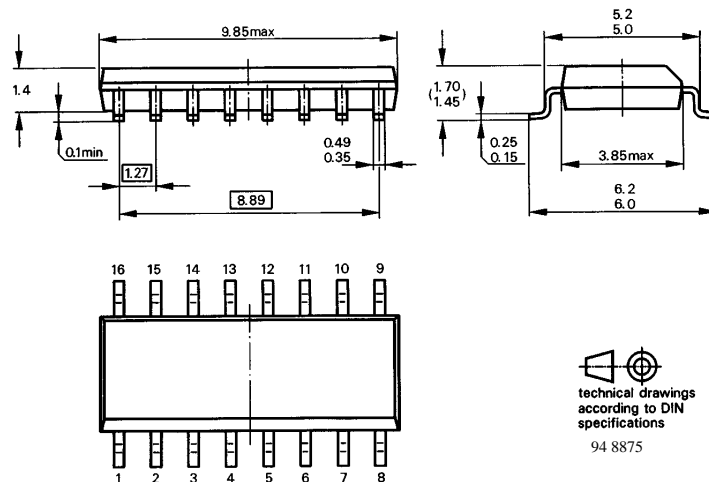
U2101B

Dimensions in mm

Package: DIP 16



Package: SO 16



Ozone Depleting Substances Policy Statement

It is the policy of **TEMIC TELEFUNKEN microelectronic GmbH** to

1. Meet all present and future national and international statutory requirements.
2. Regularly and continuously improve the performance of our products, processes, distribution and operating systems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

It is particular concern to control or eliminate releases of those substances into the atmosphere which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

TEMIC TELEFUNKEN microelectronic GmbH semiconductor division has been able to use its policy of continuous improvements to eliminate the use of ODSs listed in the following documents.

1. Annex A, B and list of transitional substances of the Montreal Protocol and the London Amendments respectively
2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA
3. Council Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

TEMIC can certify that our semiconductors are not manufactured with ozone depleting substances and do not contain such substances.

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TEMIC TELEFUNKEN microelectronic GmbH, P.O.B. 3535, D-74025 Heilbronn, Germany
Telephone: 49 (0)7131 67 2831, Fax number: 49 (0)7131 67 2423